

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Previously Amended) A digital system comprising a
2 microprocessor having an instruction execution pipeline with a
3 plurality of pipeline phases, wherein the microprocessor comprises:
4 program fetch circuitry operable to perform a first portion of
5 the plurality of pipeline phases;
6 instruction decode circuitry connected to receive fetched
7 instructions from the program fetch circuitry, the instruction
8 decode circuitry operable to perform a second portion of the
9 plurality of pipeline phases; and
10 at least a first functional unit connected to receive a
11 plurality of control signals from the instruction decode circuitry,
12 the functional unit operable to perform a third portion of the
13 plurality of pipeline phases, the third portion being execution
14 phases, wherein the first functional unit comprises:
15 first test circuitry connected to receive an operand from a
16 selected test register, and having an output for indicating a
17 condition of the operand;
18 decrement circuitry connected to receive the operand from the
19 selected test register, and having an output connected to
20 conditionally provide a decremented value of the operand to the
21 test register dependent upon said indicated condition of the
22 operand;
23 adder circuitry connected to receive a program counter value
24 and a displacement value, and having an output connected to
25 conditionally provide a branch address to a program counter
26 register dependent upon said indicated condition of the operand;
27 and

28 wherein the first test circuitry, the decrement circuitry, and
29 the adder circuitry are all operable to test the operand,
30 conditionally decrement the operand, and conditionally provide a
31 branch address to the program counter in response to a single
32 conditional branch-decrement instruction.

1 2. (Previously Amended) The digital system of Claim 1,
2 wherein the first test circuitry, the decrement circuitry, and the
3 adder circuitry are all operable to test the operand, conditionally
4 decrement the operand, and conditionally provide a branch address
5 to the program counter in response to a single conditional branch-
6 decrement instruction during a single one of the third portion of
7 pipeline phases.

3. (Canceled)

1 4. (Currently Amended) The digital system of Claim 3 1,
2 further comprising second test circuitry connected to test a
3 condition of a selected predicate register, and having an output
4 for indicating a condition of the predicate register, wherein the
5 second test circuitry is operable to inhibit the program counter
6 from receiving the branch address if the contents of the predicate
7 register do not correspond to a second condition.

Claims 5 to 9. (Canceled)

1 10. (Currently Amended) A method of operating a digital
2 system having a microprocessor with a conditional branch-decrement
3 instruction, comprising the steps of:
4 fetching a conditional branch-decrement instruction for
5 execution;

6 testing a test register selected by the conditional branch-
7 decrement instruction from among a plurality of distinct data
8 registers to determine if the contents of the test register meet a
9 first condition;
10 providing a branch address to a program counter to cause a
11 branch if the contents of the test register meet the first
12 condition; and
13 modifying the contents of the test register if the contents of
14 the test register meet the first condition.

1 11. (Previously Amended) The method of Claim 10, further
2 comprising the steps of:

3 testing a predicate register selected by the conditional
4 branch-decrement instruction to determine if the contents of the
5 predicate register meet a second condition; and

6 inhibiting the step of providing a branch address to the
7 program counter and inhibiting said step of modifying the contents
8 of the test register if the contents of the predicate register do
9 not meet the second condition.

12. (Canceled)

1 13. (Original) The method of Claim 10, wherein the steps of
2 testing, providing, and modifying are all performed during a same
3 execution phase of the microprocessor.

14. (Canceled)

1 15. (Previously Added) The digital system of Claim 1, further
2 comprising:

3 a register file including a plurality of general purpose
4 registers, each general purpose register capable of supplying an

5 operand to a functional unit and capable of receiving destination
6 data generated by a functional unit; and
7 wherein said conditional branch-decrement instruction
8 designates one of said general purpose registers as said selected
9 test register.

1 16. (Previously Added) The digital system of Claim 15,
2 further comprising:

3 second test circuitry connected to test a condition of a
4 selected predicate register, and having an output for indicating a
5 condition of the predicate register, wherein the second test
6 circuitry is operable to inhibit the program counter from receiving
7 the branch address and inhibit said step of modifying the contents
8 of the test register if the contents of the predicate register do
9 not correspond to a second condition; and

10 wherein said conditional branch-decrement instruction
11 designates one of said general purpose registers as said predicate
12 register.

1 17. (Previously Added) The digital system of Claim 16,
2 wherein:

3 said conditional branch-decrement instruction designates one
4 of said general purpose registers of a predetermined subset of said
5 general purpose registers as said predicate register.

1 18. (Previously Added) The digital system of Claim 1,
2 wherein:

3 said program fetch circuitry operable to fetch a fetch packet
4 of a predetermined plurality of instructions each first portion of
5 the plurality of pipeline phases starting at predetermined address
6 boundaries; and

7 said adder circuitry adds said displacement value to a last
8 predetermined address boundary.

1 19. (Previously Added) The digital system of claim 18,
2 wherein:

3 said instruction decode circuitry reads a predetermined bit of
4 each instruction to determine an execute packet of instructions
5 capable of execution in parallel on a plurality of functional
6 units, wherein an execute packet may include instructions in two
7 sequential fetch packets; and

8 said adder circuitry adds said displacement value to said last
9 predetermined address boundary of said fetch packet of said
10 conditional branch-decrement instruction.

1 20. (Currently Amended) The method of Claim 10, further
2 comprising the ~~step~~ steps of:

3 storing data in a register file including a plurality of
4 distinct general purpose registers;

5 recalling data from an instruction designated general purpose
6 register for supplying an operand to a functional unit;

7 storing destination data generated by a functional unit in an
8 instruction designated general purpose register; and

9 designating via the conditional branch-decrement instruction
10 one of said general purpose registers as said selected test
11 register.

1 21. (Previously Added) The method of Claim 20, further
2 comprising:

3 testing a predicate register selected by the conditional
4 branch-decrement instruction to determine if the contents of the
5 predicate register meet a second condition; and

6 designating via the conditional branch-decrement instruction
7 one of said general purpose registers as said predicate register.

1 22. (Previously Added) The method of Claim 21, wherein:
2 said step of designating said predicate register designates
3 said predicate register from a predetermined subset of said general
4 purpose registers as said predicate register.

1 23. (Previously Added) The method of Claim 10, wherein:
2 said step of fetching instructions fetches a fetch packet of a
3 predetermined plurality of instructions; and
4 said step of providing a branch address to the program counter
5 adds a displacement value to a last predetermined address boundary.

1 24. (Previously Added) The method of claim 23, wherein:
2 reading a predetermined bit of each instruction to determine
3 an execute packet of instructions capable of execution in parallel
4 on a plurality of functional units, wherein an execute packet may
5 include instructions in two sequential fetch packets;
6 dispatching each instruction of each execute packet to a
7 corresponding functional unit in parallel;
8 said step of providing a branch address to the program counter
9 adds said displacement value to a last predetermined address
10 boundary of a second sequential fetch packet if said second
11 sequential fetch packet contains said conditional branch-decrement
12 instruction.

1 25. (New) A method of operating a digital system having a
2 microprocessor with a conditional branch-decrement instruction,
3 comprising the steps of:
4 fetching a conditional branch-decrement instruction for
5 execution;

6 testing a test register selected by an operand field of the
7 conditional branch-decrement instruction to determine if the
8 contents of the test register meet a first condition;
9 providing a branch address to a program counter to cause a
10 branch if the contents of the test register meet the first
11 condition; and
12 modifying the contents of the test register if the contents of
13 the test register meet the first condition.

1 26. (New) The method of Claim 25, further comprising the
2 steps of:
3 storing data in a register file including a plurality of
4 distinct general purpose registers;
5 recalling data from an instruction designated general purpose
6 register for supplying an operand to a functional unit;
7 storing destination data generated by a functional unit in an
8 instruction designated general purpose register; and
9 designating via the conditional branch-decrement instruction
10 one of said general purpose registers as said selected test
11 register.

1 27. (New) The method of Claim 25, wherein:
2 said step of providing a branch address to the program counter
3 to cause a branch combines a displacement field of the conditional
4 branch-decrement instruction with current contents of the program
5 counter.

1 28. (New) The method of Claim 25, wherein:
2 said step of providing a branch address to the program counter
3 adds a signed displacement designated by the displacement field of
4 the conditional branch-decrement instruction to current contents of
5 the program counter.

1 29. (New) The method of Claim 25, wherein:
2 said step of providing a branch address to the program counter
3 left shifts a signed displacement designated by the displacement
4 field of the conditional branch-decrement instruction by a
5 predetermined amount and adds the left shifted signed displacement
6 to current contents of the program counter.

1 30. (New) A method of operating a digital system having a
2 microprocessor with a conditional branch-decrement instruction,
3 comprising the steps of:
4 fetching a conditional branch-decrement instruction for
5 execution;
6 testing a test register selected by the conditional branch-
7 decrement instruction to determine if the contents of the test
8 register meet a first condition;
9 providing a branch address to a program counter to cause a
10 branch by combining a displacement field of the conditional branch-
11 decrement instruction with current contents of the program counter
12 if the contents of the test register meet the first condition; and
13 modifying the contents of the test register if the contents of
14 the test register meet the first condition.

1 31. (New) The method of Claim 30, further comprising the
2 steps of:
3 storing data in a register file including a plurality of
4 distinct general purpose registers;
5 recalling data from an instruction designated general purpose
6 register for supplying an operand to a functional unit;
7 storing destination data generated by a functional unit in an
8 instruction designated general purpose register; and

9 designating via the conditional branch-decrement instruction
10 one of said general purpose registers as said selected test
11 register.

1 32. (New) The method of Claim 30, wherein:
2 said step of providing a branch address to the program counter
3 adds a signed displacement designated by the displacement field of
4 the conditional branch-decrement instruction to current contents of
5 the program counter.

1 33. (New) The method of Claim 30, wherein:
2 said step of providing a branch address to the program counter
3 left shifts a signed displacement designated by the displacement
4 field of the conditional branch-decrement instruction by a
5 predetermined amount and adds the left shifted signed displacement
6 to current contents of the program counter.